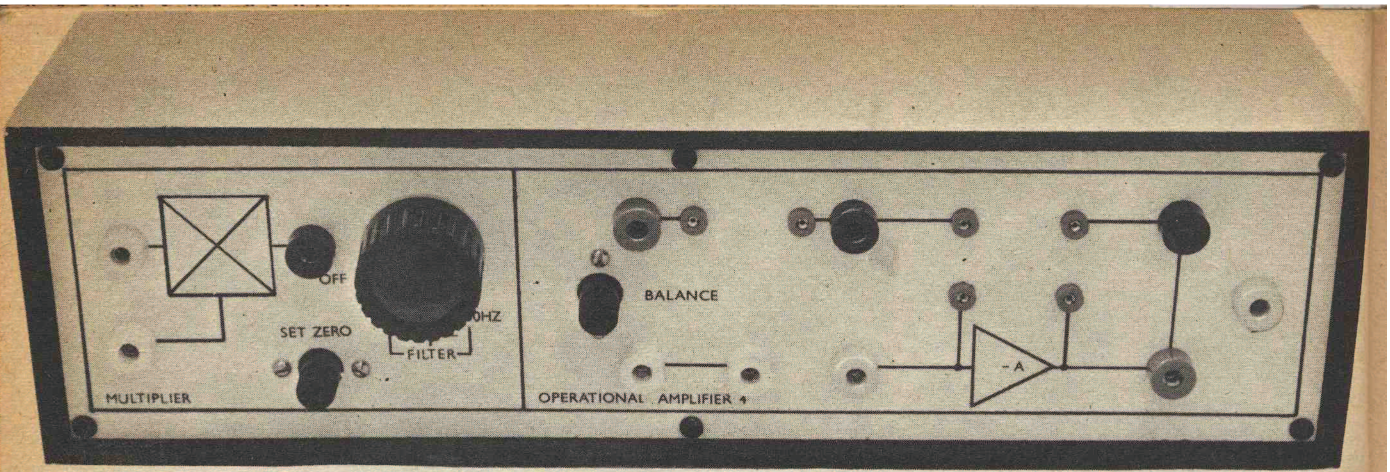


ANALOGUE COMPUTER

PEAC

By D. BOLLEN

THIS month's article deals with UNIT "D"—the multiplier, which is the final piece of PEAC equipment. After a technical description, details of the construction and setting up are given.

The servo driven potentiometer has been widely employed in the past for multiplication of one variable voltage by another, but its frequency response, in most cases, is seldom better than 0–5Hz. Modern analogue computers now tend to use all solid-state multiplier circuits, which have a frequency response extending into the kHz region, but they are both complex and expensive. Taking the quarter-square multiplier as an example, it needs five operational amplifiers and two diode function generators to produce an accurate product voltage from two inputs. It follows, therefore, that analogue multiplier circuit design can be expected to present considerable difficulties when cost is an important consideration.

UNIT "D"—THE MULTIPLIER

Working on the premise that even a multiplier of restricted performance can make a worthwhile contribution to an analogue computer which lacks such a facility, an accuracy of $\pm 2{\cdot}5$ per cent and a frequency response of 50Hz under the most favourable conditions was considered to be an acceptable specification for the UNIT "D" multiplier. Although 0–50Hz seems rather limited by ordinary electronic standards, in the context of "parallel" computer circuit operation it represents a useful compute time which compares favourably with the servo multiplier.

UNIT "D" contains three distinct circuits, two operational amplifiers and a bistable reed relay driver. One of the amplifiers is identical to those used with UNIT "A", and is available as a multi-purpose operational amplifier when the multiplier is not in service.

TIME DIVISION

With the time division multiplier, a square wave is modulated in such a way that the mark/space ratio is proportional to one input voltage, while the amplitude of the waveform is proportional to another input voltage. The mean value of the resulting waveform is then proportional to the product of the two input voltages.

Looking at Fig. 9.1, which sets out the simplified multiplier circuit with associated waveforms, a voltage E_2 is compared with a fixed voltage E_3 at the input of the integrating amplifier. A bistable relay is arranged to switch S1 and S2 when the integrator output reaches a pre-determined value, conveniently about two thirds of the maximum available amplifier output swing. If the sign of E_3 at the S1 contacts is correct, the feedback will be positive, and a self-sustained oscillation at a frequency determined mainly by E_2 and C_f will result. When $E_2 = 0$ the output from the integrator will consist of a sawtooth or symmetrical ramp waveform, with identical rising and falling slopes, which is generated by E_3.

Assume now that a voltage E_2 is applied; this will be added to, or subtracted from E_3, depending on the position of the S1 switch. The ramp waveform is therefore modified to an asymmetric form where the rising and falling slopes become dependent on the level and sign of E_2.

Waveform (a) in Fig. 9.1 depicts the asymmetric ramp for $+E_2$ and $-E_2$, while waveform (b) shows the square wave generated by the switch, of mark/space dependent on the magnitude of E_2. As S2 is synchronised with S1, so the input resistor R1 will be alternately switched to the inverting and non-inverting inputs of the product amplifier, and will remain at each contact for a time dependent on the frequency and mark/space of the switching waveform.

The amplitude of the product amplifier output is

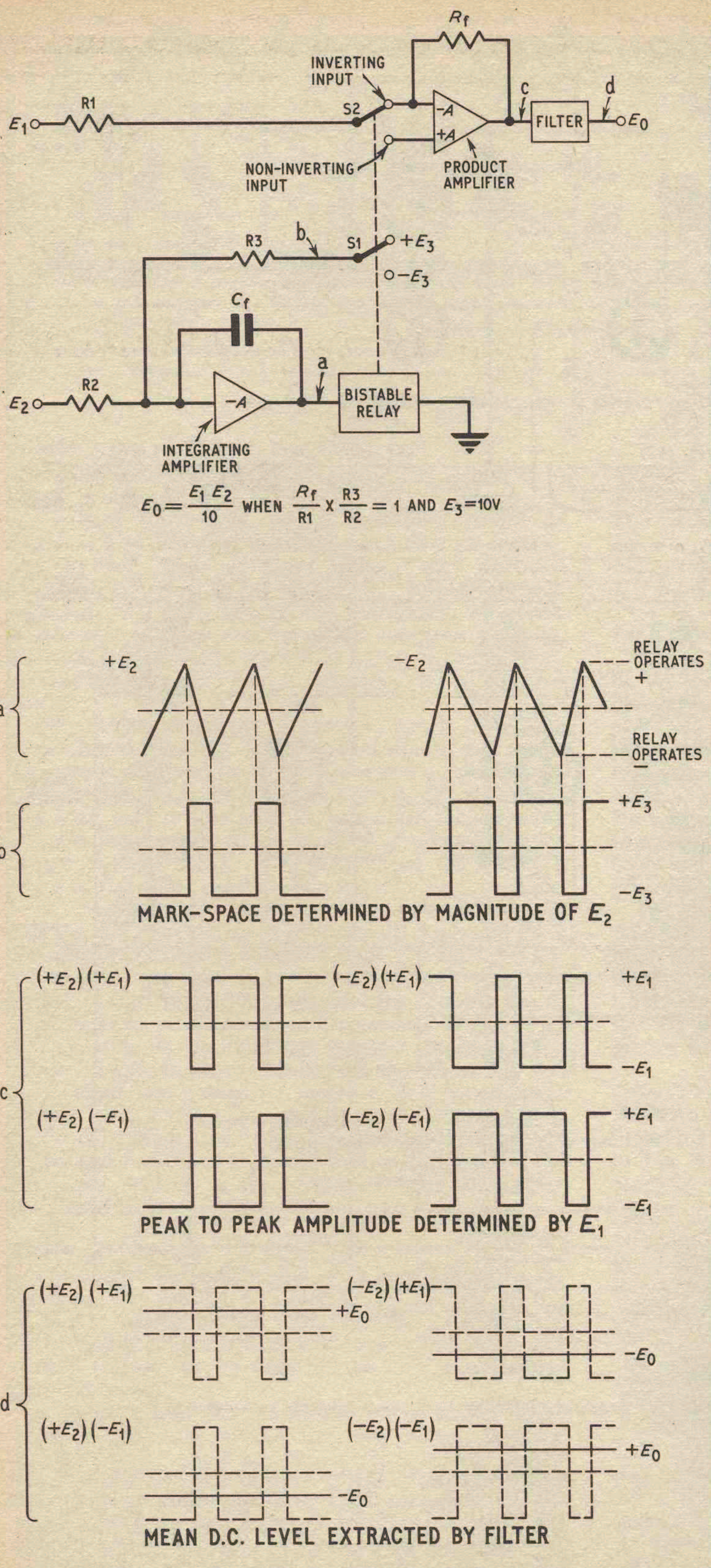


Fig. 9.1. Time division multiplier with associated waveforms

COMPONENTS . . .

UNIT "D" FRONT PANEL AND BOX

Potentiometers
VR25 100Ω wirewound
VR26 50Ω wirewound
(both panel mounting type)

Switches
S11 3 pole, 4 way rotary
S12 Double-pole slide switch (c/o contacts)

Sockets
2 red, 2 blue, 1 black, 2 yellow, 3 white, 1 green, and 6 miniature sockets

Miscellaneous
Material for front panel and box. Hardboard, 2 off 12⅜in × 4½in, 2 off 4½in × 3 3/16in. White plastic laminate, 2 off 12⅜in × 4½in, 2 off 3½in × 4½in, 1 off 12in × 3⅛in. Softwood, 25in × ½in × ½in. Knob, one Radiospares 1⅛in type PK with pointer.

UNIT "D" BISTABLE RELAY AND PRODUCT AMPLIFIER

Resistors

R1	1kΩ	*R14	10kΩ 1%
R2	4·3kΩ	R15	1kΩ
R3	4·3kΩ	R16	820Ω
R4	4·3kΩ	R17	820Ω
R5	1kΩ	R18	1kΩ
R6	100Ω	R19	8·2kΩ
*R7	11kΩ 1%	R20	22kΩ
R8	10kΩ	R21	22kΩ
R9	27kΩ	R22	8·2kΩ
R10	2·2kΩ	*R23	200Ω 2%
R11	100Ω	*R24	1kΩ 2%
*R12	10kΩ 1%	*R25	1·2kΩ 1%
*R13	9·1kΩ 1%	*R26	300Ω 1%

(All 10% ½ watt carbon composition except * = 1W metal oxide)

Potentiometers
VR1 100kΩ vertical skeleton pre-set
VR2 220Ω miniature horizontal pre-set

Capacitors
C1 1μF polyester 250V d.c.
C2 0·25μF polyester 250V d.c.
C3 1μF elect. 15V
C4 8μF elect. 15V
C5 100μF elect. 15V

Transistors
TR1, TR2 2N2926 (orange) *or* 2N3904 (2 off)
TR3 2N3906
TR4 2N3904
TR5, TR6 ACY28 *or* AC126 (2 off)

Diodes
D1–D4 OA202 (4 off)

Choke
L1 5H (Radiospares "Midget" type)

Reed coils
RLA, RLB Miniature triple 12V Osmor type MT12V (2 off)

Reed switches
RLA1, RLA2 Hamlin MRG2 20–40AT (4 off)
RLB1, RLB2

Miscellaneous
S.R.B.P., 1 off 3in × 3¼in, 1 off 3in × 4¼in. Small turret tags. Baseboard 12 in × 4in s.r.b.p. or plastic laminate

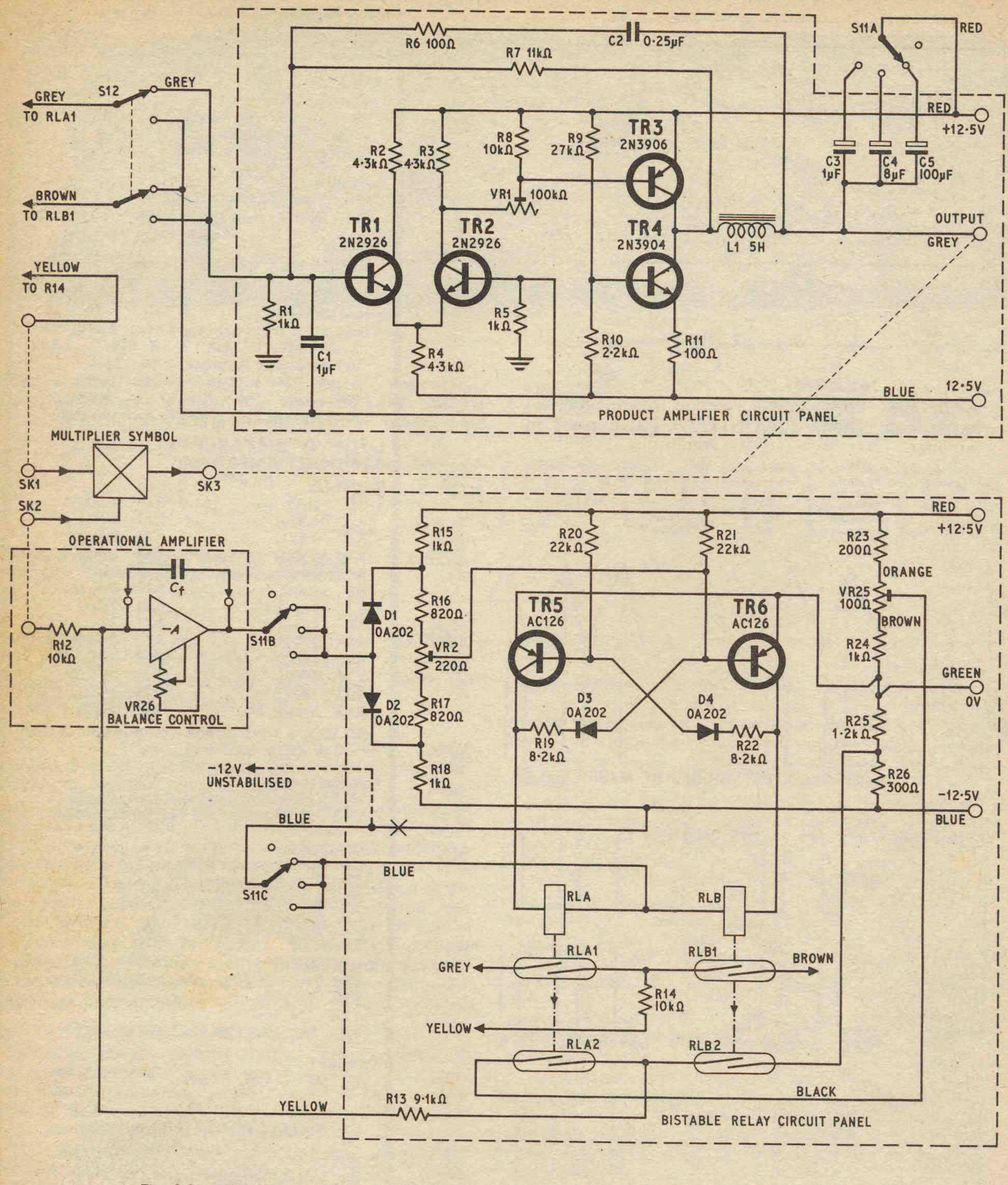


Fig. 9.2. Multiplier circuit, comprising product amplifier panel and bistable relay panel

wholly dependent on E_1, but whatever the value of E_1 it will be divided by $10/E_2$ (time division), which is the same thing as $(E_1 \times E_2)/10$, assuming of course that appropriate values for R1–R3, R_f and E_3 are chosen.

Waveforms (c) shows what happens to different signs of E_1 and E_2, in terms of the square wave. If now the mean voltage level of the output from the product amplifier is extracted by a suitable filter (see waveform (d)) it can be seen that four quadrant multiplication has been achieved. When E_1 and E_2 are both positive, or both negative, the product voltage will be positive, but when E_1 and E_2 are of opposite sign, the product becomes negative.

The multiplier circuit will now be described.

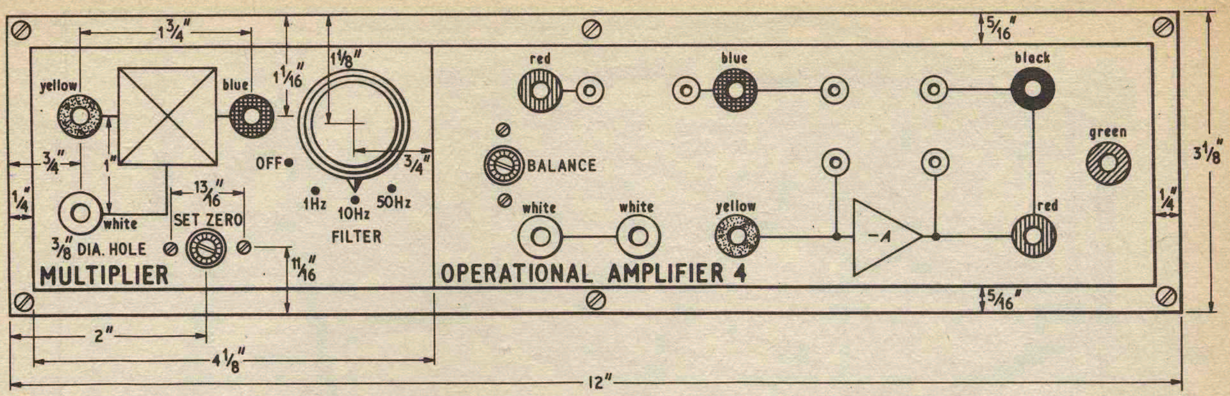


Fig. 9.3. Dimensions and engraving details for UNIT "D" front panel

UNIT "D" MULTIPLIER CIRCUIT

As the operational amplifier circuit has already been given in connection with UNIT "A", it appears in symbolised form only in the multiplier circuit of Fig. 9.2, with VR26 as the front panel balance control, and a fixed value of input resistor R12 provided internally for use with the multiplier. As the feedback capacitor C_f only affects the integrator waveform frequency, without altering other multiplier characteristics, it is useful to leave it as a plug-in component, so that the multiplier carrier frequency can be adjusted easily.

The output from the integrator, which it will be remembered from Fig. 9.1 carries information as to the magnitude and sign of input E_2, is fed via S11B to a diode resistor network composed of D1, D2, R15–R18, and VR2, the purpose of which is to allow the following bistable relay driver to be switched at precisely determined voltage levels. VR2 establishes the working point of the diode resistor network.

A conventional cross-coupled multivibrator is utilised as a relay driver, with reed coils RLA and RLB forming the respective collector loads of TR5 and TR6. D3 and D4 are used to ensure a "cleaner" switching action at high repetition rates, and the bistable circuit will function satisfactorily at frequencies in excess of 100Hz without undue relay contact bounce. The reference voltage, which was shown as $\pm E_3$ in Fig. 9.1, is extracted from a resistor network R23–R26 and VR25 in Fig. 9.2. VR25 allows positive and negative values of E_3 to be made equal. E_3 voltages are then fed, via RLA2 and RLB2 switches, and resistor R13, back to the summing junction of the integrator, thus completing the closed-loop to maintain oscillation.

SIGN CHANGE

The square wave switching cycle is presented to the input of the product amplifier by RLA1 and RLB1, with R14 acting as the input resistor. Changeover switch S12 is included to allow the sign of the multiplier output voltage to be changed to suit a particular problem set-up.

A product amplifier open-loop gain of about 1,000, which is the gain of the Fig. 9.2 circuit, is quite satisfactory for good accuracy when working with a fixed, closed-loop gain close to unity. Long-tailed pair TR1 and TR2 provide inverting and non-inverting inputs, while TR3 is the output transistor, and TR4 forms a constant current load for TR3, in place of a fixed resistor, thus enabling larger loads to be driven without excessive dissipation. VR1 serves to zero the amplifier output.

The ratio of resistors R7 and R14 gives a product amplifier gain (closed-loop) of 1·1, while R13/R12 yields an equivalent gain for the integrating amplifier of 0·91. The lower value of gain for the integrator enables E_2 to equal E_3 without stopping the integration cycle, and yet the overall gain of the multiplier is still unity because $1{\cdot}1 \times 0{\cdot}91 = 1$.

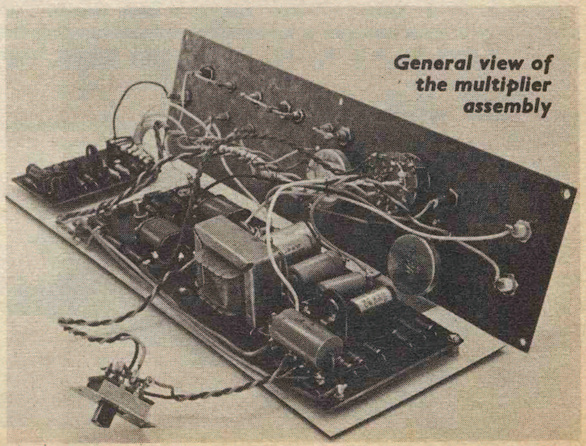
FILTER CIRCUIT

The purpose of the filter circuit L1, C2–C5, R6, and S11A, is to remove the square wave carrier without distorting the product waveform when input voltages are time varying. Bearing in mind that computer waveforms are extremely diverse, it is almost impossible to achieve near perfect results with one filter circuit, especially when the carrier frequency is not far removed from input frequencies. To allow compromise, therefore, the cut-off frequency of the Fig. 9.2 filter can be set by switch S11A to suit the circumstances of a particular problem set-up.

The three switch positions, 1Hz, 10Hz, and 50Hz, represent approximately the roll-off points given by the filter, and the bandwidth handled by the multiplier. In the 1Hz position the filter will virtually eliminate carrier ripple when input voltages are of very low frequency, but the 50Hz setting is used with fast integrator waveform inputs, where ripple may be less objectionable.

CONSTRUCTION OF UNIT "D" FRONT PANEL AND BOX

Details of the UNIT "D" front panel and box appear in Fig. 9.3 and Fig. 9.4. Note that the operational amplifier (OA4) socket positions and panel markings



General view of the multiplier assembly

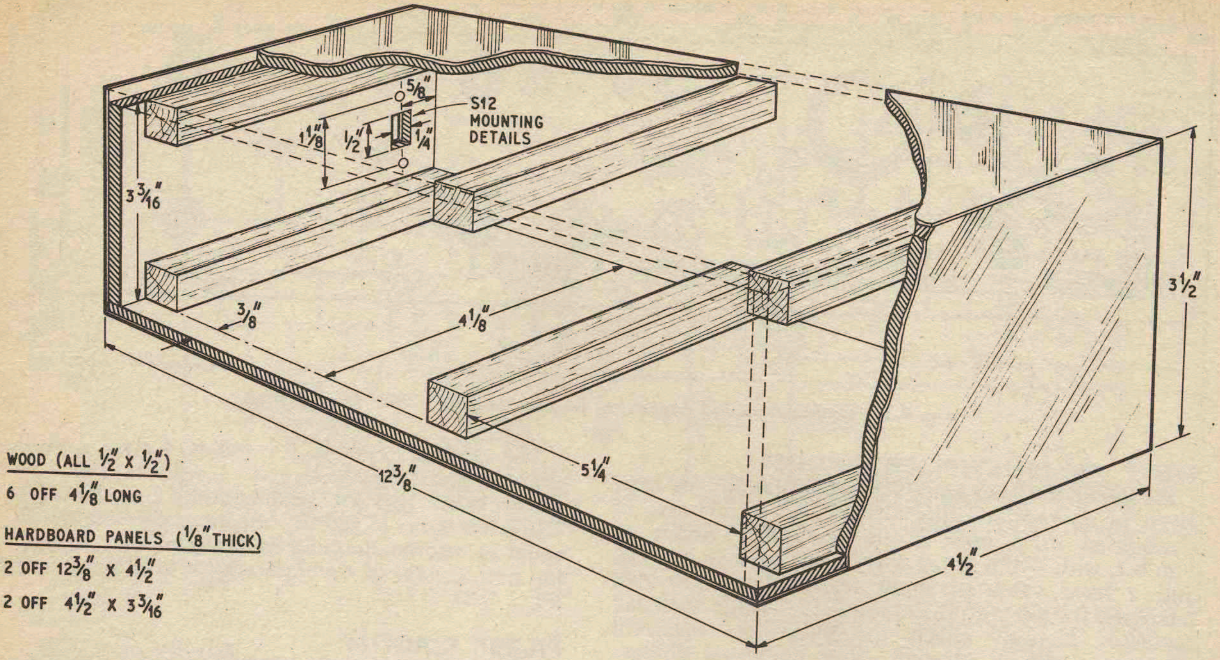


Fig. 9.4. Construction of the box for UNIT "D"

are the same as for UNIT "A" operational amplifiers. S11, VR25, VR26, and all sockets may be mounted after the front panel has been marked and drilled.

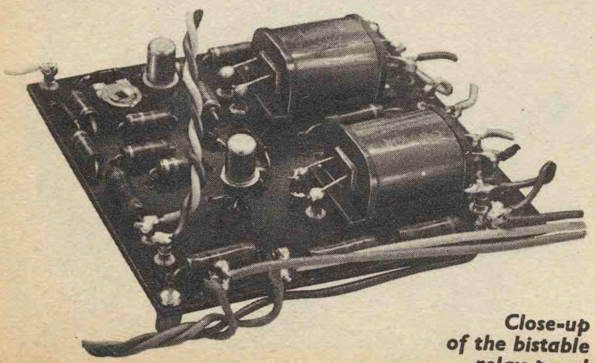
INTERNAL LAYOUT OF THE MULTIPLIER

The internal layout and interconnecting wiring of the multiplier are shown in Fig. 9.5. Operational amplifier, bistable relay driver, and product amplifier circuit panels are bolted with stand-off spacers to a 12in × 4in s.r.b.p. or plastics laminate baseboard, which rests on the wooden bearers at the base of the UNIT "D" box.

Component placement positions for the bistable relay circuit panel, and the product amplifier panel, also appear in Fig. 9.5, together with a rear view of the front panel assembly. The operational amplifier (OA4) is made up in accordance with instructions given in the May issue of PRACTICAL ELECTRONICS (pages 209–210).

BISTABLE RELAY CIRCUIT CONSTRUCTION

Drill the bistable relay circuit panel according to Fig. 9.6, and insert turret tags. Then mount all components and complete underside wiring, leaving the reed switches RLA1, RLA2, RLB1, and RLB2 until last. A triple reed coil is specified for the Fig. 9.2 circuit, to allow the addition of an extra pair of reed switches if the multiplier is to be enlarged to cater for three input voltages; this modification will, of course, also involve the construction of another product amplifier.



Close-up of the bistable relay panel

PRODUCT AMPLIFIER CIRCUIT CONSTRUCTION

Drilling details and underside wiring of the product amplifier panel appear in Fig. 9.7. Accurate matching of input transistors TR1 and TR2 may not be necessary with this low gain circuit. A 2N2926 transistor should not be employed in the TR4 position, in place of the 2N3904, as its maximum V_{ce} will be exceeded.

After inserting turret tags, mount resistors and transistors first, then follow with L1, and capacitors C2–C5. C1 is soldered into position last of all, across the amplifier input turret tags, as shown in Fig. 9.5.

FINAL ASSEMBLY AND SETTING UP OF UNIT "D"

Mount the three circuit panels on the baseboard and complete all interconnecting wiring between the circuit panels and the front panel, including S12 which can be left floating for the time being. The resulting assembly can be set-up and tested out of its box.

Connect red, green, and blue flexible wires from the bistable relay panel to the UNIT "A" power supply solder tags, or alternatively to TL1, TL2, and TL3 with stackable plugs.

Place S11 in the "off" position and zero-set the operational amplifier (OA4) following instructions given earlier for UNIT "A" amplifiers, after allowing the usual warm-up period. When adjusting the VR26 balance control connect M/SK2 to any earth socket with a patching lead. Next, attach a sensitive d.c. voltmeter (0–1V) to M/SK3 and zero-set the multiplier output by adjustment of VR1 on the product amplifier circuit panel.

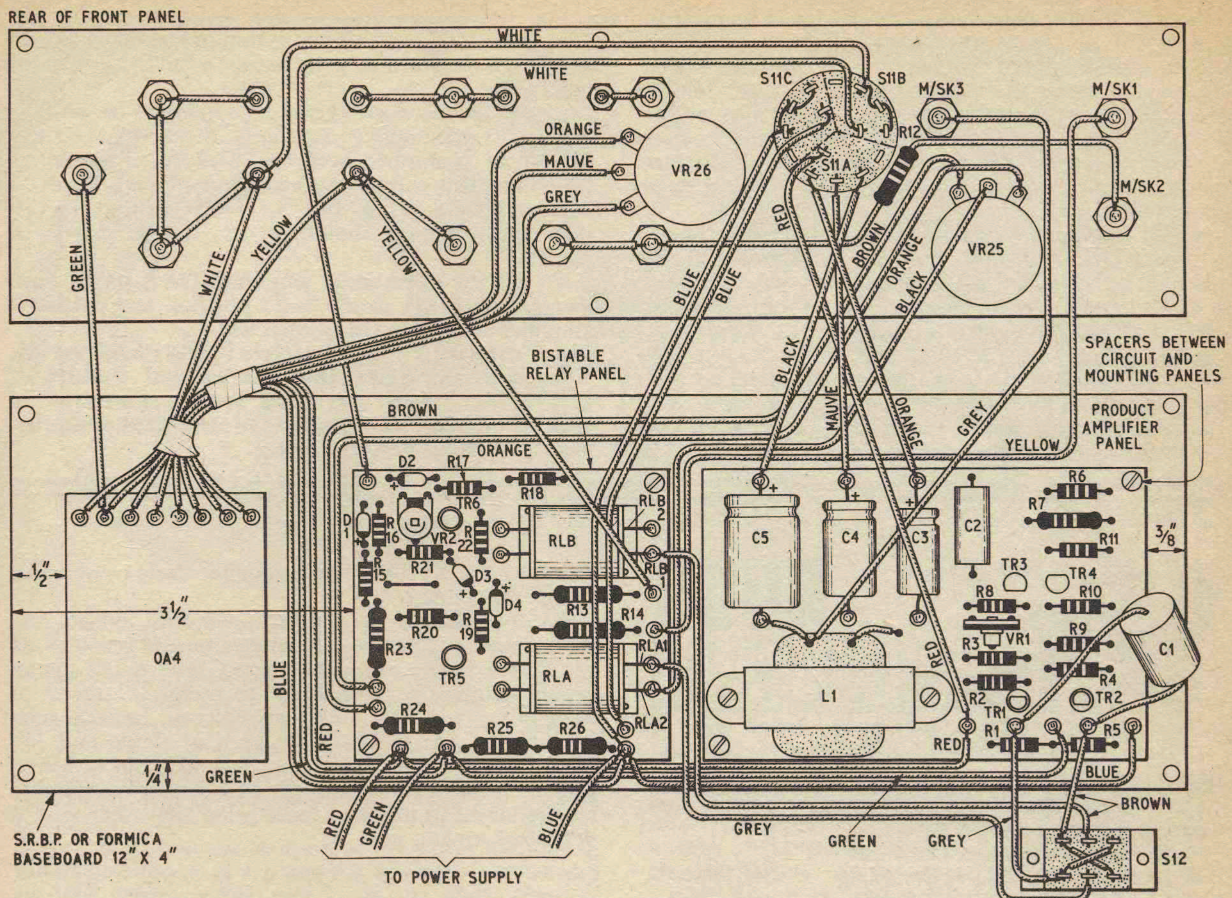
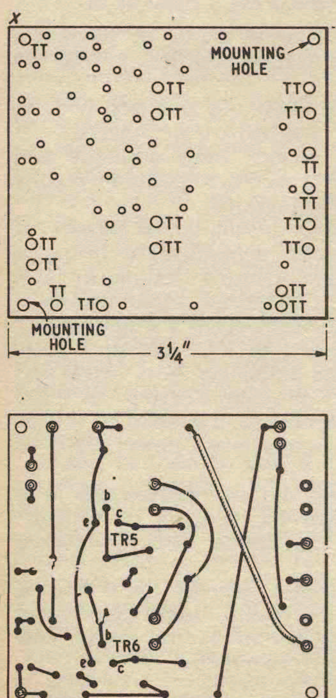


Fig. 9.5. Internal layout and wiring of UNIT "D" multiplier



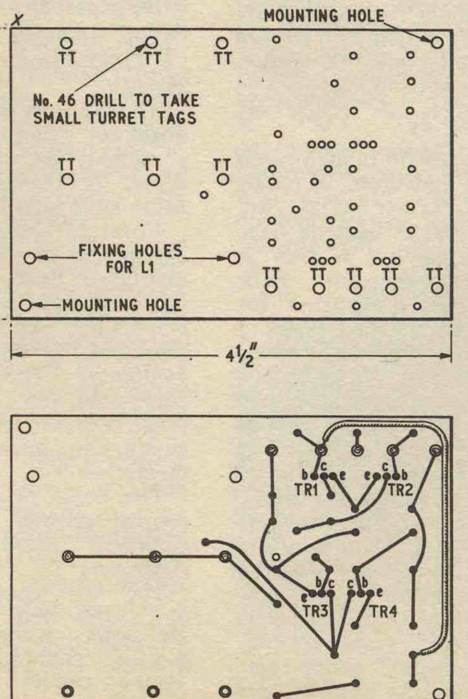


Fig. 9.6 (far left). Top and underside views of bistable relay panel

Fig. 9.7 (left). Top and underside views of product amplifier circuit panel

Insert a 0·25μF capacitor into OA4/SK11 and SK12, and switch S11 to 10Hz. A "buzz" from the relays should now be heard, which may or may not sound erratic. Transfer the d.c. voltmeter to OA4 output while the relays are still working and adjust VR2 on the bistable relay panel for zero volts; this should produce an even note from the relays. Return the voltmeter lead to the multiplier output M/SK3 and this time zero-set with VR25.

Apply an input of +5V to M/SK2; the relay "buzz" will drop in frequency, but no output should be observed at M/SK3. Transfer the +5V patching lead to M/SK1 and again no output should be seen. Finally, apply +5V to both inputs, M/SK1 and SK2, to produce a multiplier output of $5^2/10$ or 2·5V.

Throw switch S12 to change output polarity and experiment with inputs of differing sign. If all is well, the product voltage should retain its value of 2·5 for any sign combination of input voltages and S12.

For best accuracy it is advisable to go over all adjustments again to obtain optimum settings, and also verify that the multiplier will handle a full range of input voltages.

Due to the fact that the power supply may be working close to its maximum current limit, there could be some fall-off in multiplier accuracy because of switching transients, this can be checked by employing the extra current facility, S1 in Fig. 3.1. The optional −12V relay power supply should obviate the difficulty if it occurs.

To use the operational amplifier (OA4) on its own, merely switch S11 to the "off" position and patch the amplifier sockets in the normal way.

Next month: The final article in the PEAC series. This will complete the operational details of UNIT "D", and will give some examples of special circuits to represent mechanical phenomena, and some general notes.